#17 IDS 4/1/04

Docket No.: 4363P004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Arash Hassibi, et al.	Examiner: Quang D. Vu
Application No: 09/843,486	Art Unit: 2811
Filed: April 25, 2001	
For: OPTIMAL SIMULTANEOUS DESIGN AND FLOORPLANNING OF INTEGRATED CIRCUIT	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Request for Continuation. It is respectfully requested that the cited information be considered and that the enclosed copy of the PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Match and Return

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10/29/03

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Janice Shannon — 10/29/2003 / 10-29-03

Janice Shannon — *Date*